Thursday Afternoon, October 18, 2007

Manufacturing Science and Technology

Room: 615 - Session MS-ThA

MEMS Manufacturing

Moderator: R. Ghodssi, University of Maryland

2:20pm **MS-ThA2 Double-Exposure Gray-Scale Technology for Improved Vertical Resolution of 3D Photoresist Structures**, ***L.A. Mosher***, University of Maryland, *B.C. Morgan*, U.S. Army Research Laboratory, *R. Ghodssi*, University of Maryland

We report the development of a new double-exposure gray-scale photolithography technique to batch fabricate three-dimensional structures in photoresist with improved vertical resolution. Deep reactive ion etching is used to transfer the patterned photoresist into silicon, enabling a complete three-dimensional microfabrication platform with many applications for MEMS devices, such as lenses and microengines. Gray-scale photolithography utilizes a photomask to spatially control the ultraviolet light intensity incident on a photoresist layer. This control is achieved by diffraction through sub-resolution pixels on the mask using projection photolithography. Projection optics keep only the zeroth order intensity, preventing the higher-order diffractions from reaching the wafer. The local pixel size is correlated to the transmitted intensity and therefore determines the height in photoresist after development. Vertical resolution, determined by the number of available pixels, is limited by the mask vendor. Current mask fabrication techniques allow for tens of pixel sizes, which is insufficient for some MEMS applications. We introduce a double-exposure gray-scale technique, utilizing two gray-scale exposures prior to a single development. In this technique, two pixel sizes are used with two partial exposures, resulting in a third unique photoresist height after development. By using all pixel combinations, we achieved an exponential increase in the number of available levels. Our initial test design utilized only eight pixel sizes, but realized 64 unique height levels in photoresist after development. We created an empirical model to correlate the pixel combination and exposure times with the photoresist height, which facilitates the design of pixel layouts for nearly arbitrary geometries. This model was used to optimize the exposure times to minimize the average and maximum vertical step height. We fabricated a seventeen-pixel test structure based on this model and observed a significant improvement over single-exposure. A decrease in the average vertical step height from 0.19 µm to 0.03 µm was achieved as well as a decrease in the maximum vertical step height from 0.63 µm to 0.24 µm. Detailed modeling parameters and experimental results from double-exposure gray-scale structures will be presented.

2:40pm **MS-ThA3 MEMS Manufacturing in a High Volume CMOS Wafer Fabrication Facility**, ***G.D. Winterton***, Texas Instruments Inc. **INVITED**

The original concept of the digital micromirror device (DMD) is a far cry from the current embodiment of today's devices. Design, process, and packaging innovations of the past decade have enabled Texas Instruments Digital Light Processing (DLP) devices capable of transitioning from on to off over 5000 times a second with native contrast ratios in excess of 4000:1. TI's philosophy is to manufacture the DLP MEMS device in an existing high volume CMOS wafer fab. This philosophy constrains the MEMS processes to be compatible with existing CMOS processes. Sharing the facility with standard CMOS allows TI to benefit from the economies of scale which exist in a high volume CMOS fab. The MEMS group has a dedicated team of development, integration, and process engineers embedded within the larger fab engineering organization. This facilitates synergy between the engineering teams and leverages the experiences of the larger organization. MEMS manufacturing has additional requirements not found on standard CMOS. Most MEMS are 3D devices requiring very tight control of film thicknesses to control the spacing between MEMS elements. Film stresses are of much greater concern in MEMS processing which has required additional control methodologies to be put in place to facilitate much tighter control than standard CMOS. TI DLP products utilize sacrificial photoresist layers to create the spacings between the MEMS elements. Standard lithographic tools and techniques are used to create the patterns and traditional plasma etching are used to define these features. The metal deposition process cannot use traditional sputter etch techniques due to the presence of photoresist on which the metal is being deposited onto. The metal must also be deposited at low temperatures to avoid resist reticulation. Photoresist stripping and cleaning techniques had to be developed which could integrate into the fab without affecting the sacrificial resist layers or inducing unwanted topography. Special care is paid to surface conditions to avoid stiction effects since metal-to-metal elements cone in direct contact during device operation. The final step prior to packaging is the plasma removal of the sacrificial resist layers to release the MEMS elements. Significant engineering effort has been dedicated to packaging since particles are a major source of defects. Control of the internal package environment is an area of special concern to control stiction during the lifetime of the product.

3:40pm **MS-ThA6 Manufacturing Challenges and Method of Fabrication of On-Chip Capacitive Digital Isolators**, ***P. Mahalingam***, *D. Guiling, S. Lee, R. Figueroa, W. Tian, Y. Patton, I. Khan*, Texas Instruments

Digital isolators permit high-speed data transmission in industrial and process control applications which involve hazardous voltage environments. Texas Instruments introduced on-chip capacitive isolation technology for digital isolated couplers which enables products to provide isolation voltage up to 7000Vrms and ~12000V surge capability. An innovative, robust method of manufacturing low noise, 10kV peak on-chip capacitive digital isolator integrated in a BiCMOS process flow is presented this paper. Silicon based on-chip capacitive isolators used here are fabricated in a high performance precision analog 5V, 0.3um digital CMOS process with extremely low noise performance, and uses a lightly doped bulk, p-type substrate. Electrical measurements of on-chip capacitors reported here follow UL 1577, IEC 60747-5-2, and CSA standards. These include two tests (a) ramped voltage test from 4kVrms to 10kVrms to force device breakdown, which would quantify highest allowable overvoltage (VIOTM) , and (b) pulsed constant voltage test where 50 short pulses of 8kV and higher (to force breakdown) at 1us intervals are applied to device under test (DUT) for both polarities of the device, bottom-injection and top-injection. In this work, on-chip capacitors used for high voltage isolation is built using a dielectric stack which is a combination of pre-metal oxide, and/or the various dielectrics from metal-1 to top-metal depending on whether the bottom electrode is moat or metal-1. The choice of dielectric employed in these capacitors is based on the results of a I-V measurement study which examined electrical breakdown voltage of various dielectric materials such as silicon nitride, silicon oxynitride, oxides such as HDP, TEOS at various film stresses. Silicon nitride and oxynitride have the best isolation properties and offer unique advantages in meeting the isolation capacitor requirements. The challenges of integrating silicon nitride and oxynitride films as part of a dielectric stack in CMOS metallization scheme, the influence of the order in which these films are deposited in the dielectric stack on isolation capacitor's BVrms capability, pulse voltage performance, and device reliability are discussed. A model is developed to optimize dielectric film stresses in order to ensure isolation capacitor manufacturability by allowing wafer warpage to be maintained lower than the regime in which stepper chucking errors occur during downstream lithography processes.

4:00pm **MS-ThA7 A Novel Crystallized Silicon Thin Film Transistor Based Piezoresistive Cantilever Label Free Biosensor**, ***C. Zhan***, *P. Schuele, J. Conley, J. Hartzell*, Sharp Laboratories of America, INC.

This paper reports a novel integrated biosensor based on the piezoresistive effect of laser crystallized silicon (c-Si) thin film. The sensor is comprised of a c-Si resistor integrated on a PECVD SiO2 cantilever using low temperature surface micromachining techniques. Once the cantilever is deflected mechanically, the electrical response of the integrated thin film resistor changes accordingly. The fabrication and measurement results of crystallized silicon thin film resistor on a cantilever are presented. Our unique laser crystallized a-Si film enables a high quality thin film piezoresistor be accommodated on a small and thin cantilever using MEMS surface micromachining techniques. The integrated piezoresistive cantilever transducer can be selectively functionalized and implemented in large arrays for biosensing applications. The device consists of a c-Si thin film resistor embedded in a PECVD SiO2 cantilever. The air gap between the cantilever and the substrate is defined by a PECVD a-Si sacrificial film, which was removed during release etch step. When the cantilever is deflected by an external force, pressure or surface stress, a uniaxial strain is induced along the longitudinal direction of the cantilever. The strain stretches or compresses the thin film resistor and therefore changes the resistance. The fabrication process is a standard TFT process flow compatible surface micromachining process. Only two extra masks, one for sacrificial mesa patterning and another for cantilever outline patterning, are introduced to the standard TFT flow to realize the c-Si TFT based piezoresistive cantilever biosensor. A 1.5 um thick a-Si is PECVD deposited as the sacrificial film and a TMAH based release etchant is used to release the MEMS cantilever. The PECVD SiO2 films of the standard TFT process are used to form the body of the cantilever. One design of the

cantilever is 140um long, 50um wide and 0.5um thick. The c-Si TFT active thin film is used to form the piezoresistor. The thickness of the active c-Si piezoresistor is 100nm. Initial tests on our fabricated MEMS piezoresistive biosensors confirm the piezoresistive effect. External mechanical actuation tests were performed using a micropositioner for calibration. The minimum detectable cantilever deflection is 3nm at 3dB signal to noise ratio. Currently, the sensitivity of the fabricated cantilever biosensor is 3.07uv/nm. The biosensing tests are on the way and results will be updated.

4:20pm **MS-ThA8 Divergence in N/MEMS and Semiconductor Manufacturing**, ***J.D. Evans***, Defense Advanced Research Projects Agency (DARPA) **INVITED**

Nano and Micro Electro-mechanical System (N/MEMS) technology seeks to build small devices (nano/milli scale features) using processing equipment similar to that utilized in the semiconductor industry. Because of similarities in scale and equipment, the performance and potential growth of N/MEMS, as an industry, has been often compared to the growth of the semiconductor industry. However, similarity of length scale and fabrication equipment is not sufficient to ensure similar market performance. In fact, the MEMS and semiconductor industry face dramatically different technical and market dynamics that cause one to question whether this comparison can allow one to draw any meaningful conclusions. In this talk, the author will focus on four fundamental differences between N/MEMS and semiconductor industries: (1) difference in scalability (with implications for a "Moores' Law for MEMS"), (2) difference in process diversity, (3) difference in manufacturing volume, and (4) differences in required fabrication precision (N/MEMS requires higher fabrication precision than semiconductors). These differences suggest that N/MEMS industry faces a fundamentally different set of technical and market constraints than faced by semiconductor industry, and lead one to expect a fundamentally different market evolution. While they do not diminish the fundamental importance of N/MEMS technology, the differences do suggest a need for N/MEMS specific expertise in evaluating and exploiting N/MEMS opportunities, and may suggest a need for a new set of fabrication technologies specifically designed for the N/MEMS markets. DARPA Distribution Statement "A": Approved for Public Release, Distribution Unlimited.

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