Electronic Materials and Processing

Room: 612 - Session EM-WeM

Contacts, Interfaces and Defects in Semiconductors

Moderator: L.M. Porter, Carnegie Mellon University

8:00am **EM-WeM1 Role of Hydrogen Bonding Environment in Amorphous Silicon Films for Passivation of Crystalline Silicon Based Photovoltaic Devices**, *M.Z. Burrows, U.K. Das,* ***R.L. Opila****, R.W. Birkmire*, University of Delaware

The search for an ideal surface passivation layer of crystalline silicon (c-Si) to be employed in the silicon heterojunction photovoltaic device has garnered much attention. The leading candidate is a few nanometers thick amorphous silicon (a-Si:H) film. This is due to the fact high open circuit voltages above 700mV, key to 20% power conversion efficiencies, are only possible with low surface recombination velocities at the passivated c-Si / a-Si interface. Our approach involves a concentrated effort to link the deposition parameters to the thin a-Si:H material properties as revealed with Fourier transform infrared spectroscopy (FTIR) and match observed changes in H bonding to passivation quality as determined by effective minority carrier lifetime measurements. Reported dependencies of film surface passivation quality on substrate preparation, orientation, and deposition temperature have been extended in this work to include H to SiH_4 dilution ratio and post-deposition annealing. Marked differences have been observed with carrier lifetimes ranging from few microseconds to few milliseconds. A simple yet extremely sensitive FTIR procedure based on Brewster angle transmission measurements enables the probing of films of just 5-10nm thickness. By cataloguing the changes in H content and bonding environment as hydrogen dilution or annealing conditions were varied a comprehensive picture of material quality as related to passivation quality has emerged. Simple avoidance of the growth regimes that lead to epitaxial growth of Si on the c-Si substrate produces decent lifetimes on the order of 500μsec can be achieved. However this often entails harsh deposition conditions that lead to defective films of primarily bulk SiH_2 bonding. Subsequent low temperature anneals, presumed to only relax the amorphous lattice, are shown to not only cause unexpected bulk hydrogen evolution but also involve various complex reactions. Annealing in atmosphere changes surface SiH_2 to chainlike $(SiH_2)_n$ as well as oxygen back-bonding to create surface oxides like $SiH(O_3)$. Annealing in vacuum causes minimal surface SiH_2 disturbance but rather surface SiH and SiH_3 evolution. Finally it is concluded that the best passivation layer consists of primarily well ordered mono-hydride bonding in purely amorphous phase. Sub-optimal amorphous phase films can be improved by post-deposition anneal.

8:20am **EM-WeM2 Impact of Intrinsic Vacancies on Phase Change and Epitaxial Growth of In_2Se_3 on Si(111)**, ***C.Y. Lu****, E.N. Yitamben, T.C. Lovejoy,* University of Washington*, K.M. Beck, A.G. Joly,* Pacific Northwest National Laboratory*, M.A. Olmstead, F.S. Ohuchi*, University of Washington

The strong change in optical reflectivity during the amorphous-crystalline phase transition in ternary chalcogenides is the basis of re-writeable compact disc and digital video disk technology. The binary, group-III-chalcogenide semiconductor, In_2Se_3 has recently been proposed as a resistance-based phase-change random access memory (PRAM) material due to its large (10^5) resistance change between the crystalline and amorphous phases.[1] The intrinsic vacancies and structural variability characterizing crystalline In_2Se_3 likely play an important role in controlling phase-change characteristics. We have investigated growth of amorphous and epitaxial In_2Se_3 films on Si(111), as well as the crystallization of amorphous In_2Se_3 films through resistive annealing using a combination of scanning tunneling microscopy, photoemission spectroscopy, and X-ray diffraction. Amorphization of crystalline In_2Se_3 films by laser annealing was studied using photo electron emission microscopy. Despite the 7.3% lattice mismatch, we are able to grow laminar, epitaxial films of γ- In_2Se_3 (0001) up to at least 3 nm in thickness that exhibit a surface reconstruction associated with the ordered vacancy structure; we attribute this ability to grow laminar films to the flexibility provided by the intrinsic vacancy structure. A minimum thickness of 2 bilayers (0.64 nm) is required to undergo the phase change and a minimum thickness of 3 bilayers (0.96 nm) is required for the ordered-vacancy reconstruction characteristic of the epitaxially grown material during phase change. Annealing room-temperature-deposited films can transform amorphous In_2Se_3 to be highly textured γ- In_2Se_3 with the (0001) plane parallel the substrate surface. A buffer layer of epitaxial In_2Se_3 before deposition of the amorphous film lowers the crystallization temperature and improves the uniformity of the crystalline In_2Se_3 phase. This work was supported by NSF grant DMR 0605601. TCL acknowledges support from NSF/NCI IGERT DGE-0504573. Some of the research was pursued at the Advanced Light Source, which is supported by the DOE under contract DE-AC02-05CH11231. KMB acknowledges the support from U.S. Department of Energy by Battelle Corporation.

[1] H. Lee, D-H. Kang, and L. Tran, Mat. Sci. Eng. B 119 (2004) 196.

8:40am **EM-WeM3 Reliability of Electrical Contacts to Single Crystal SiC**, ***R.S. Okojie***, NASA Glenn Research Center **INVITED**

The utilization of Silicon Carbide (SiC) semiconductor-based microsystems targeted for extreme applications (i.e., high temperature, high power, extreme vibration, and aggressive chemical environments) has largely been hindered by intrinsic material defects and the reliability issues that are associated with the stability of the contact metallization.[1] In this talk, the research efforts at NASA Glenn to resolve the reliability problems of the contact metallization will be presented, which includes the in-depth reliability studies to identify the multilayer metallization that provides stable long-term performance of ohmic contact to SiC. The observation of process-induced stacking faults (SFs) has also been determined to present a reliability problem to 4H-SiC polytype devices. The formation of single and multiple stacking faults that sometimes give rise to 3C-SiC was observed in several doped n-type 4H-SiC epilayer following thermal oxidation. Transmission electron microscopy following oxidation revealed double stacking faults and bands of 3C-SiC in the 4H-SiC epilayer. Depth-resolved cathodoluminescence spectroscopy at 25 oC based on low energy-excited electron nanoscale luminescence revealed a spectral peak at 2.5 eV photon energy that was not present in the sample prior to oxidation. This is in addition to the 3.22 eV photon energy peak corresponding to 4H-SiC.[2] The polytypic transformation is attributed to the motion of Shockley partial dislocations on the (0001) slip planes.[3] Auger electron spectroscopy, Scanning Electron Microscopy, Transmission electron microscopy, and current-voltage measurements that were used to develop an in-depth knowledge of these failure mechanisms will be discussed.

[1]P. G. Neudeck, R. S. Okojie, Liang-Yu Chen, Proceedings of the IEEE, Vol: 90 , Issue: 6 , pp.1065 . 1076. 2004

[2]R.S. Okojie, D. Lukco, L. J. Brillson S. Tumakha, G. Jessen, M. Xhang and P. Pirouz,. Appl. Phys. Lett. 79, 3056 (2001).

[3]Robert. S. Okojie and Ming Zhang, in Silicon Carbide 2004-Materials Processing and Devices, edited by Michael Dudley, Perena Gouma, Tsunenobu Kimoto, Philip G. Neudeck, and Stephen E. Saddow (Mater. Res. Soc. Symp. Proc. 815, Warrendale, PA , 2004).

9:20am **EM-WeM5 Epitaxial CVD of Metallic HfB2 on SiC Substrates**, ***Y. Yang***, University of Illinois at Urbana-Champaign*, V.M. Torres,* Dow Corning Compound Semiconductor*, J.R. Abelson*, University of Illinois at Urbana-Champaign

HfB2 is an attractive candidate for many technological applications owing to its refractory melting temperature (3250°C), high mechanical hardness (29 GPa), low electrical resistivity (15 μΩ-cm), high optical reflectivity, and chemical inertness at high temperatures. The epitaxial growth of HfB2 is particularly interesting because the (0001) plane has a small lattice mismatch with the compound semiconductors GaN (1.5%) and SiC (-2%) and the coefficients of thermal expansion are reasonably close for these three materials. In principle, epitaxial HfB2 could be used as a growth template and/or as an electrical contact in a multilayer compound semiconductor device while maintaining crystallographic continuity. We report that high quality HfB2 thin films can be deposited on SiC(0001) substrates by chemical vapor deposition using the single source precursor Hf(BH4)4. This precursor is a solid which sublimes at room temperature with a vapor pressure of 15 Torr, such that no carrier gas or heated delivery lines are needed; and it contains no organic or halogen groups. The HfB2 microstructure is strongly dependent on temperature. Films deposited at low substrate temperature are (0001) textured and polycrystalline, as indicated by SEM and XRD analysis. An increase of deposition temperature increases the grain size and reduces the mosaic spread. Films deposited under optimal deposition conditions are extremely flat. The (0001) rocking curve has a FWHM of only 0.26°, indicating a very high epitaxial quality. The room temperature resistivity is < 20 μΩ-cm, close to the bulk value. The surface morphology of the epitaxial film is sensitive to the surface finish of the SiC substrate: film coalescence can be delayed by substrate surface imperfections.

9:40am **EM-WeM6 Surface and Grain Boundary Electron Scattering in Encapsulated Cu Thin Films**, ***T. Sun***, *B. Yao*, University of Central Florida, *V. Kumar*, Carnegie Mellon University, *A.P. Warren, K.R. Coffey*, University of Central Florida, *K. Barmak*, Carnegie Mellon University

Surface and grain boundary electron scattering contribute greatly to resistivity as the dimensions of polycrystalline metal thin films and interconnects are reduced to and below the length of the electron mean free path. A quantitative measurement of the relative contributions of surface and grain boundary scattering to the resistivity is very challenging, requiring not only the preparation of suitably small conductors having independent variation of the two relevant length scales, namely, the sample critical dimension and the grain size, but also independent, experimental quantification of these two length scales. Since for most work to date the sample grain size has been either assumed equal to conductor dimension or measured for only a small number of grains, the quantification of the classical size effect still suffers from an uncertainty in the relative contributions of surface and grain boundary scattering. A methodology is reported to independently evaluate surface and grain boundary scattering in dielectric encapsulated polycrystalline Cu thin films. The film resistivity measured at both room temperature and at 4K is compared for samples having different grain sizes (determined from 400 to 1,500 grains per sample) and film thicknesses. The experimental data is compared to existing and empirical models of surface and grain boundary scattering in thin films. The resistivity measured at room temperature and 4K is observed to follow similar trends. We find that the resistivity contribution from grain boundary scattering to be significantly greater than that of surface scattering for Cu thin films having Cu/SiO_2 surfaces and grain sizes similar to their thickness. We also find that the resistivity at room temperature is not equal to the simple sum of the low temperature resistivity and the room temperature phonon resistivity contribution, suggesting that either Matthiessen's rule can not be applied, or that the grain boundary and/or surface scattering has a temperature dependence.

10:40am **EM-WeM9 Microstructural Evolution of Nickel Germanides in the $Ni_{1-x}Ta_x$/Ge Systems during In-situ Annealing**, ***J.W. Lee***, *J.H. Bae, M.H. Park, H.B. Kang, H. Kim, C.W. Yang*, Sungkyunkwan University, Korea

It is becoming increasingly difficult to further improve the performance of Si-based complementary metal-oxide-semiconductor (CMOS) using traditional device scaling. Ge-based devices have attracted considerable attention for high-performance logic applications on account their its lower effective mass and high carrier mobility (double for electrons and four times higher for holes compared with those in Si).[1] However, the NiGe shows a poorer thermal stability than NiSi. The limited thermal stability of NiGe may deteriorate the performance improvement of Ge metal-oxide-semiconductor field-effect transistors (MOSFETs). These features of Ge substrate motivated us to investigate the mechanism of the formation and thermal stability of NiGe and the effect of alloying elements, i.e. the tantalum which is the refractory metal. In this study, the formation and morphological evolution of the germanides formed from the $Ni_{1-x}Ta_x$ (~30nm)/Ge (x=0 and 0.1) systems as a function of temperature was investigated by in-situ annealing in the transmission electron microscope (TEM, JEM-3011, JEOL Co. Ltd) with a specimen heating holder. The sheet resistance of the germanides formed in the $Ni_{0.9}Ta_{0.1}$/Ge system was lower at temperatures above 550°C than the Ni/Ge system. Through the addition of Ta atoms, Ni germanide grain growth was retarded and the surface morphology of the Ni germanide layer improved. An approximately 10nm thick Ta-rich layer formed on the top of the germanide layer. Eventually, the agglomeration of Ni germanide was retarded and the thermal stability of the Ni germanide formed from the Ni-Ta alloy became superior to that formed from the pure Ni.

[1] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. Mclntyre, and K. C. Saraswat, IEEE Electron Dev. Lett. 23, 473 (2002).

11:00am **EM-WeM10 Probing the Effect of Interaction and Thermal Expansion Mismatch between Ge and Templated Mask on Defects during Selective Molecular Beam Epitaxy of Ge on Si**, ***D. Leonhardt***, *Q. Li, S.M. Han*, University of New Mexico

We have previously demonstrated that high-quality, single-crystalline Ge can be grown on Si by epitaxial lateral overgrowth (ELO) as well as by touchdown where nanoscale windows (~7 nm in diameter) are created through a thin chemical SiO_2 layer. These techniques have been successfully used to reduce threading dislocations in the Ge-Si lattice mismatched system. Despite the improvement, dislocations are generated in the epilayer above the templated mask. To test the hypothesis that these defects occur due to varying level of epilayer-template interaction energy (e.g., bond strength and diffusion activation barrier) and thermal expansion differences between the epilayer and template, in addition to coalescence events, we have created masks of SiO_2, Al_2O_3, and Ta having thermal expansion coefficients smaller, larger, and equal to Ge epilayers selectively grown on Si in the mask openings. The windows in the masks are created by spin-coating a disperse layer of polystyrene spheres on the Si substrate followed by mask deposition and lift-off. Ge islands are selectively grown in the mask openings using molecular beam epitaxy (MBE), and further grown laterally over the mask until coalescence occurs. The Ge layers are then characterized by x-ray diffraction, transmission electron microscopy, and etch pit density after chemical-mechanical polishing to determine the effect of interaction energy and thermal expansion differences on the resulting film quality. Furthermore, we quantitatively measure the desorption activation energy of Ge adspecies from the SiO_2, Al_2O_3, and Ta masks to determine the characteristic diffusion lengths of Ge adspecies on the mask surfaces. We will then present the impact of inter-distance of windows in the masks on dislocation density in the Ge epilayer.

11:20am **EM-WeM11 Silver-Bearing Ohmic Contacts for AlGaN/GaN Heterostructures**, ***M.A. Miller***, *S.E. Mohney*, The Pennsylvania State University

We have investigated the use of Ag in place of Au in V- and Ti-based ohmic contacts to $Al_{0.27}Ga_{0.73}N$/GaN heterostructures for high electron mobility transistors. An optimized V/Al/V/Ag contact provided a specific contact resistance of $1.7x10^{-6}$ Ohm-cm^2 when annealed at 825°C for 60s in N_2. As measured by atomic force microscopy, the contacts had a root-mean-square roughness of 4.5 nm over a 10 x 10 micron area, which was much smoother than the analogous Au-bearing metallizations. An optimized Ti/Al/Ti/Ag contact provided a higher minimum specific contact resistance of $7.4x10^{-6}$ Ohm-cm^2, and the Ti/Al/Ti/Ag contacts were not as smooth as the V/Al/V/Ag contacts, perhaps due to the higher annealing temperatures necessary to minimize the resistance of the Ti-based contacts. The specific contact resistance and morphology of the V/Al/V/Ag contacts were also superior to those of the more conventional Ti/Al/Ti/Au and V/Al/V/Au contacts tested. Transmission electron microscopy revealed a very limited reaction of the annealed V/Al/V/Ag metallization with the semiconductor, leaving the AlGaN layer intact. The majority of the AlGaN interface is contacted by Ag-bearing phases. Silver has a lower work function than Au and may facilitate the formation of a low-resistance ohmic contact.

11:40am **EM-WeM12 Schottky Barrier Characteristics and Interfacial Reactions of Ir and Ti Gate Metallizations on In0.52Al0.48As/In0.53Ga0.47As High Electron Mobility Transistors**, ***L. Wang***, *I. Adesida*, University of Illinois at Urbana-Champaign

InAlAs/InGaAs HEMTs are promising devices for high speed circuits, millimeter-, and sub-millimeter-wave applications. Selection of gate metallizations plays a significant role in the performance, operation mode, stability, and manufacturability of these devices. Two factors need to be considered in choosing gate metals, namely, work function and reactivity with InAlAs during fabrication and operation. Electrically, metal work function determines Schottky barrier height (φB) which in turn decides key device operation parameters such as threshold voltage, transconductance, gate capacitance, etc. Structurally, reactivities or diffusivities of metals/InAlAs control the final gate-channel distance and thermal stability of the transistors. However, a thorough correlation of electrical and structural characterizations of metal/InAlAs contacts at various annealing conditions is still lacking. In this study, we examined the relationship between the φB characteristics and interfacial reactions of Ti/InAlAs and Ir/InAlAs. I-V characteristics of Schottky diodes were used for φB and ideality factors characterizations. Cross-sectional transmission electron microscopy is utilized to elucidate the microstructural evolution occurred at the metal/semiconductor interfaces. For Ir/InAlAs, φB decreased slightly compared to the as-deposited value when annealed at 250 °C. Beyond that φB increased monotonically until it reached the peak value of 825 meV at 400 - 425 °C. Further increasing the temperature led to φB degradation. Over a wide temperature range from ~375 to 450 °C, φB of over 800 meV could be achieved. XTEM studies showed that enhancement in φB is due to the formation of amorphous layer at the interface. Annealing above 455 °C led to the nucleation of IrAs2 crystals. For Ti/InAlAs, as-deposited diodes had a typical φB of 668 meV and an ideality factor of 1.0. Two maxima in φB were observed for samples annealed at temperatures above 300 °C. The first set of maxima had values between 748 and 726 meV. The second set of maxima had higher φB of over 760 meV after prolonged annealing. Similar to Ir/InAlAs, an amorphous mixture between Ti and InAlAs formed for samples annealed at short durations. Prolonged thermal treatment resulted in aggressive reaction leading to Kirkendall voids formation, deformation of InAlAs, and TiAs crystal growth. Such aggressive reaction and thus defects formation led to higher diode ideality factors.

12:00pm **EM-WeM13 Improvement of AlGaN/GaN HEMT and GaN Schottky Contact Device Performance by Reduction of Epitaxial Film Dislocation Density**, ***D.J. Ewing***, *M.A. Derenge, P.B. Shah, U. Lee, T.S. Zheleva, K.A. Jones*, Army Research Lab

The electrical characteristics of AlGaN/GaN high electron mobility transistors (HEMTs) and GaN Schottky contacts were correlated with dislocations and other material defects. AlGaN/GaN heterostructures and GaN epitaxial films were grown using conventional MOCVD and pendeo-epitaxy (PE), a lateral growth technique that reduces the dislocation density of the epitaxial films by 2-3 orders of magnitude. Current-voltage (I-V) and capacitance-voltage (C-V) measurements were conducted to determine the quality of the Ni gate (Schottky) contacts to both the conventional and PE films. The Schottky contacts to the PE material all displayed a single, homogeneous Schottky barrier height evidenced by the linearity of the log I-vs-V plot over 4-5 orders of magnitude. Conversely, the Schottky contacts to the conventional material displayed an inhomogeneous Schottky barrier height, with a characteristic "knee" at low voltage indicating the presence of a low Schottky barrier height. The average ideality factor increased from 1.71 for the PE material to 2.29 for the conventionally grown GaN. The average reverse leakage current increased from $7.5x10^{-4}$ A for the PE GaN to = $4.0x10^{-3}$ A for the conventionally grown GaN. The electrical properties were then correlated with improved material quality as determined by several microscopy techniques. The conventional GaN epitaxial films were found to have an RMS surface roughness twice as large as that of the PE film. Similarly, cathodoluminescence revealed that the near band edge intensity of the PE films was almost an order of magnitude higher than the conventionally grown material, indicating the presence of fewer defects in the PE material. Devices fabricated on the AlGaN/GaN heterostructure also displayed variations in electrical properties. Variations in the ideality factor, Schottky barrier height, and reverse leakage current density were 1.60-2.60, Φ_B=0.60-0.95 eV, and J=$1x10^{-4}$-$1x10^{1}$ A/cm^2, respectively. These variations correlated with a variation in local etch pit density directly under the gate contact as determined by SEM. For devices with high leakage-current density, the etch-pit density was found to be twice as high as that of devices with low leakage current density. Determining the relationship between the electrical characteristics and materials defects will facilitate the fabrication of high-power and high-frequency devices with improved performance and reliability.

Authors Index

Bold page numbers indicate the presenter