Thursday Afternoon, October 18, 2007

Electronic Materials and Processing

Room: 612 - Session EM-ThA

High-K/High Mobility Substrates and Power Electronics

Moderator: C. Eddy, Naval Research Laboratory

2:00pm EM-ThA1 Growth and Characterization of III/V Compound Semiconductors on Silicon, *S.F. Cheng, R.L. Woo, **L. Gao**, R.F. Hicks*, University of California, Los Angeles
III-V materials are promising materials for high speed, low power devices in next-generation integrated circuits. However, a roadblock to implementing these materials in integrated circuit applications is the heteroepitaxial growth of III-V on silicon. Here, we have developed a process flow for the selective-area metalorganic vapor-phase epitaxy (MOVPE) of GaAs on Si (100) substrates. Arsenic passivation was demonstrated in the reactor environment at a temperature of 650 °C. The subsequent deposition of GaAs was carried out in a two-step process, with nucleation at 250-550 °C and second-step growth at 630 °C. High-resolution x-ray diffraction of films nucleated at 350°C or below exhibited polycrystalline grains, whereas films nucleated at 400 °C and above were single crystal. A clear c(4×4) LEED pattern of GaAs deposited on a blanket Si substrate is demonstrated for the first time. Growth on patterned Si indicates improved crystallinity as determined by XRD and plane-view TEM. The photoluminescence of SA-MOVPE GaAs on Si is shown to be nearly identical to homoepitaxial GaAs. The potential of these materials for the fabrication of high-speed devices will be discussed at the meeting.

2:20pm EM-ThA2 STM Imaging of Selective Bonding of Hf, O, and HfO_2 on InAs(001)-(4x2)/c(8x2), *J.B. Clemens, A.C. Kummel*, University of California, San Diego
Hafnium oxide (HfO_2) has been successfully used as a high-κ gate oxide on Si(100) and is being investigated as a high-κ gate oxide for high mobility III-V semiconductors. To form an electronically passive interface on a III-V semiconductor is challenging because the bonding to the group III and group V atoms must be distinct to leave both atoms in their bulk oxidation states with an unchanged electronic structure. The bonding of Hf, O, and HfO_2 on the InAs(001)-(4x2)/c(8x2) surface was probed with scanning tunneling microscopy (STM) to determine the exact bonding positions at low coverage. The InAs(001)-(4x2) surface is advantageous for these studies since it has a row and trough structure with In atoms at the center of the rows and As atoms at the edges of the rows which are easy to image in STM. Furthermore, the InAs(001)-(4x2) surface contains no As-As dimers so surface atoms are rarely displaced during oxide and oxygen dosing. Although the sticking probability for O_2 on this surface is very low (~0.015%), it is found that O_2 bonds preferentially to the first layer undercoordinated In rows. This is consistent with O-metal bond formation being thermodynamically more favorable than As-O bond formation. Furthermore, the As atoms on the edge of the row have only half-filled dangling bonds so they are poor electron donors and less likely to react with oxygen than As dimer atoms found on other III-V reconstructions. Conversely, STM shows that Hf bonds initially to the second-layer tricoordinated As atoms along the edges of the In rows of the InAs(001)-(4x2) surface. This is consistent with the Hf atoms donating electrons to the unfilled dangling bonds of the second layer tricoordinated As atoms. In order to investigate the bonding geometry of HfO_2 on the InAs(001)-(4x2) surface, Hf and O_2 are co-deposited. Current work will show the result of annealing these surfaces in order to create ordered submonolayer coverages of HfO_2.

2:40pm EM-ThA3 Materials and Process Needs for Power Electronic Integration, *K.D.T. Ngo, G.Q. Lu,* Virginia Tech, *P. Chow*, Rensselaer Polytechnic Institute **INVITED**
A typical switched-mode converter contains semiconductor, conductive, magnetic, dielectric, and thermal-management elements. The wide variations in materials and processes employed to make these components, the large dimensions, and the requirements for low losses have limited the chance for integration. *** The integration strategy pursued divides the power electronic converter into three building blocks: Active, Passive, and Filter Integrated Power Electronics Modules (AIPEM, PIPEM, and FIPEM). Electro-magneto-thermal structures are described for realization of the functionalities expected from the structures. Materials and processes have been identified to verify the operation of the integrated structures. While the entire converter cannot be integrated using current technologies, the equipment and process steps to fabricate the three types of IPEMs are similar. *** The AIPEM structure (e.g., an "embedded-power" module) contains the semiconductor devices, the associated ancillary functions (e.g., gate drives, sensing, and protection), and thermal management elements (e.g., heat spreader, heat sink, and micro-channel coolers). Interacting with the AIPEM to shape the conversion gain is the PIPEM (e.g., an integrated inductor/capacitor/transformer network) containing passive components designed to propagate energy at the switching frequency. The FIPEM (e.g., an integrated lossy transmission line for EMI filtering), on the other hand, contains passive components designed to attenuate at the switching frequency, or the frequencies beyond the useful power bandwidth. *** Semiconductor materials employed include silicon, silicon carbide, and gallium nitride. Nano-material technology has been developed for bonding and interconnects, and multiferroic nano-composites for passive integration. Other common metals, polymers, and ceramics are also used. *** Exemplified processes include "Metal Post Interconnected Parallel Plate Structure," "Flip Chip on Flex," "Dimple-Array Interconnect," and "Embedded Power." Sputtering, plating, etching, spin-coating, screen-printing, tape casting, sintering, and solder reflowing are typical process steps. New materials and processes are needed for high yield and reliable operations under wide ranges of temperature, fields, vibration, pressure, and other environmental conditions.

3:40pm EM-ThA6 DFT Molecular Dynamics Simulation of Ge-O-Al Selective Bond Formation at the a-Al2O3/Ge(001) Interface, *E.A. Chagarov, A.C. Kummel*, University of California, San Diego
Density-Functional Theory simulations of interface formation between amorphous Al2O3 oxide and Ge(001)-(2x4) surface were performed to model the chemical bonding at the oxide-semiconductor interface. A realistic DFT sample of amorphous Al2O3 was developed using "melt and cool" hybrid Classical-DFT Molecular Dynamics (MD) approach. Initially, 24 samples of 100 atoms were prepared by classical MD runs by melting initially crystalline sample. The spatial distribution of the atoms in each sample was quantified using Radial Distribution Functions (RDF), coordination distribution, and average coordination number. The sample with an atomic spatial distribution closest to the experimental geometry was DFT annealed to obtain a more realistic fully relaxed DFT geometry. The DFT annealed a-Al2O3 sample was placed on a 8 layer Ge(001)-(2x4) slab and partially relaxed for 200 steps with the fixed Ge atoms allowing the a-Al2O3 to adjust to Ge surface topography and to form oxide-Ge bonds. Subsequently, the top 5 layers of Ge were unfrozen, and the whole a-Al2O3-Ge system was annealed, cooled and relaxed to form a-Al2O3-Ge interface. DFT simulations of a-Al2O3-Ge interface revealed that during annealing, Al atoms migrate out of interface, while O atoms migrate into the interface. The bonding of a-Al2O3 to Ge occurs mainly through O atoms forming a low density Al-O-Ge bonds to the Ge dangling bonds on the surface. It was found that several O atoms diffused into Ge bulk forming interstitials. Electronic structure analysis of the interface demonstrated that Density of States (DOS) of the interface region was approximately a superposition of a-Al2O3 and Ge(001)-(2x4) DOS curves without significant new features. The oxygen-rich a-Al2O3/Ge interface is consistent with Al forming stronger bonds to O than to Ge and with experimental results. The small changes in electronic structure for a-Al2O3/Ge interface formation are consistent with the oxide reducing the number of Ge dangling bonds and only forming a low density of weakly ionic Al-O-Ge bonds.

4:00pm EM-ThA7 Band Alignments of Y2O3 on Different Group IV Substrates, *S.Y. Chiam,* Imperial College London, UK, *W.K. Chim,* National University of Singapore, *A.C. Huan,* Institute of Materials Research and Engineering, Singapore, *J. Zhang,* Imperial College London, UK, *S.J. Wang, J.S. Pan,* Institute of Materials Research and Engineering, Singapore, *S.G. Turner*, Imperial College London, UK
Band alignment is an important property for oxides-semiconductor lineup especially for MOS devices. Band offsets for many oxides-semiconductor has and can be predicted by charge neutrality level (CNL) model (gap states model). This model however is based on an essentially "bulk" phenomenon of gap states dipoles. There have been, however, differences in the measured valence band offsets (VBO) and conduction band offsets (CBO) of oxides (especially rare-earth oxides) and the predicted offsets from the CNL model. In this work, we present the experimental data for rf-sputtered Y2O3 on Si, Ge, strain-Si, strain-SiGe and relaxed SiGe. The virtual substrates were grown by GSMBE. Some of these substrates expect differences (based on various sources, investigating changes in conduction and valence band) in the valence and conduction band of less then 0.1eV. However, the VBO and CBO between the oxide and these substrates amounts often to >0.5eV. In addition, we have pre-sputtered a thin mono-

layer of Y metal before deposition of the Y2O3 (in-situ). This reduces the valence band offset for the films on all the substrates. This can be explained by changes in either interface structure and/or chemical nature at the interface (dipoles). Our work shows the importance of the nature at the interface in determining the offsets between an oxide and semiconductor.

4:20pm EM-ThA8 High-k/III-V Integration: from GaN to InSb, *P.D. Ye*, Purdue University **INVITED**

The principal obstacle to III-V compound semiconductors rivaling or exceeding the properties of Si electronics has been the lack of high-quality, thermodynamically stable insulators on GaAs (or on III-V materials in general). For more than four decades, the research community has searched for suitable III-V compound semiconductor gate dielectrics or passivation layers. The literature testifies to the extent of this effort with representative, currently active approaches including sulfur passivation, silicon interface control layers (Si ICLs), in situ molecular beam epitaxy (MBE) growth of Ga2O3(Gd2O3), ex situ atomic layer deposition (ALD) growth of Al2O3 and HfO2, jet vapor deposition (JVD) of Si3N4, ALD, PVD or MBE of HfO2 + Si or Ge ICL, Al2O3 plasma nitridation or AlN passivation. The research on ALD approach is of particular interest, since the Si industry is getting familiar with ALD Hf-based dielectrics and this approach has the potential to become a manufacturable technology. In this talk, the authors will review some of our previous work on integration of ALD high-k dielectric Al2O3 on GaAs, InGaAs and GaN, and demonstration of high performed depletion-mode III-V MOSFETs. But for very large scale integrated (VLSI) circuits or high-speed digital applications, enhancement-mode (E-mode) III-V MOSFETs within the Si CMOS platform are the real devices of interest. We will discuss on the detailed CV measurements (high frequency-low frequency CV, Quasi-static CV, split-CV, and photo-CV) on high temperature annealed ALD Al2O3 and HfO2 dielectrics on GaAs and InGaAs. InGaAs includes In0.2Ga0.8As/GaAs, In0.53Ga0.47As/InP and other In-rich InGaAs materials. We will focus on some new results on inversion-type E-mode NMOSFET fabricated on p-type In0.53Ga0.47As, and InP surfaces using ALD Al2O3 and HfO2 dielectrics. The maximum inversion current of ~ 400 mA/mm and Gm of ~ 130 mA/mm and the middle gap interface trap density Dit of low 10x11/cm2-eV to 2x1012/cm2-eV is achieved at these material systems. We will also briefly report on some new CV results on high-k/InSb surface. The work is in close collaborations with G.D. Wilk, Y. Xuan, H.C. Lin, Y.Q. Wu, T. Shen, T. Yang, Z. Cheng, A. Lochtefeld, J. Woodall, M. Lundstrom, M.A. Alam, R.M. Wallace, J.C.M. Hwang, A. Liu, W. Wang, M. Santos. We also would like to thank B. Yang, M. Hong, R. Kwo, H. Gossmann, K.K. Ng, J. Bude and others who contributed significantly at the initial stage of this research.

5:00pm EM-ThA10 Study of High-κ Dielectrics on InGaAs for CMOS Applications, *F.S. Aguirre-Tostado, C. Hinkle, K.J. Choi, M. Milojevic, S.J. McDonnell, J. Kim, M.J. Kim, E. Vogel, R.M. Wallace*, University of Texas at Dallas

Scaling and performance of integrated circuits has been pushed to the limit where the substitution of Si itself by higher mobility channel materials. Bulk electron mobilities for GaAs and InGaAs are well above those obtained for Si. At room temperature, the electron mobility of InGaAs exceeds the 10,000 cm^2/V-s making this material a good candidate for high-performance logic applications. In this paper we will describe chemical, structural and electrical properties of high-κ dielectrics on InGaAs channels. The chemistry and structural properties of LaAlO$_3$, HfAlO$_3$ and HfO$_2$ on InGaAs will be presented using in-situ XPS and LEISS analysis as well as HRTEM and XRD analysis. The thermal stability for relevant thermal budgets associated with dopant activation in a surface channel MOSFET InGaAs based device is examined in view of the electrical characteristics of MOS capacitors. This work is supported by the MARCO MSD Focus Center.

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