Electronic Materials and Processing

Room: 612 - Session EM-FrM

Hf-based Dielectrics and Their Interfaces

Moderator: R.L. Opila, University of Delaware

8:00am **EM-FrM1 Electrical Properties of High k Dielectrics Improved by Atomic Scale Nitrogen Depth Profile**, ***W.J. Maeng***, *H. Kim*, POSTECH in Korea

Nitrogen incorporation produces several benefits in the performance of high k gate oxides. However, since too much nitrogen incorporation at the interface of gate dielectric can result in device degradation, the atomic scale control of nitrogen depth profile is desirable. In this study, we have improved the electrical properties of gate oxides, including dielectric reliability and interface state density, by depth profile control using in situ nitrogen incorporation during plasma enhanced atomic layer deposition (PE-ALD). The PE-ALD HfO_2 films with oxygen plasma and PE-ALD HfO_xN_y films with N/O mixture plasma were prepared at various growth conditions, changing nitrogen profile (bottom, middle and top) and N/O flow ratio (from 0 to 4). The best electrical properties in terms of hysteresis, EOT, and interface state density were obtained when the nitrogen was incorporated in the middle of the thin film with the N/O ratio of 2, which has not been achievable by other nitridation techniques. The EOT and interface state density of middle nitridation sample was reduced to 0.95nm (HfO_2 : 1.10nm) and $0.75x10^{11}cm^{-2}eV^{-1}$ (HfO_2 : $1.20x10^{11}cm^{-2}eV^{-1}$). Also, the 50% failure electric field was improved from -10.3 MV/cm to -12.2 MV/cm.

8:20am **EM-FrM2 Effect of Annealing Temperature on the Chemical Composition, Chemical Depth Profile,and Film Morphology of High-k Gate Dielectrics by AR-XPS and AFM**, ***G. Conti***, *G. Peydaye, C.C. Wang, T. Sato, Y. Uritsky, S. Hung, P. Liu*, Applied Materials

Hf-based films are alternative gate dielectric films to SiON because of their high dielectric constant and their relatively wide band gap. These films should stay amorphous after activation annealing at T>1000 °C because grain boundaries may serve as paths of dopant diffusion. Pure HfO2 is not a good gate dielectric film because it crystallizes at a low temperature of 500 °C. In this work the effect of different annealing temperatures on chemical composition, and atomic depth profile of HfSiON films is studied by AR-XPS, AFM and TEM. HfSiON films with different N concentrations were annealed at temperatures ranging from 500C to 1050C. These films are thermally stable up to T=1000°C. AR-XPS analysis shows that Hf concentration remains constant, while the N concentration increases linearly with decoupled plasma nitridization power (DPN). All the samples show one layer of HfSiON on Si substrate with thickness of about 20Å. The AR-XPS depth profile shows that Hf and N are evenly distributed in the films, and carbon is observed as a contaminant element on the film surface. The film roughness by AFM is RMS=2Å. The temperature of T=1050C is most commonly used in the CMOS processes, because it is the temperature of Si recovery after dopants implantation. At this temperature the film should remain amorphous and thermodynamically stable. The set of films previously studied, was then annealed at T=1050C. AR-XPS analysis shows that the concentrations of both Hf and N drop significantly, while the N concentration still increases as the DPN power increases. The resulting films consist of two stacked layers of SiOx/HfSiON/Si whose total thickness ranges between of 24Å and 36Å. The AR-XPS depth profile shows that Hf is closer to the Si interface, N is buried in the middle of the film and a significant fraction of carbon is present both in the surface and in the bulk. These AR-XPS results can be explained only if crystallization occur. TEM images show the appearance of micro islands. AFM analysis shows that the film roughness increases by a factor of 20 compared to that of the film annealed at T=1000C. Based on the high film roughness, we conclude that AR-XPS technique on films at T=1050C produces meaningless results in term of composition and depth profile data. However, increasing the amount of N in the film prevents film crystallization. These films show a relative low roughness, and the AR-XPS results are similar to those of the samples annealed below T=1000C.

8:40am **EM-FrM3 Suppression of Ge-N Bonding at Ge-HfO_2 and Ge-TiO_2 Interfaces: Deposition on Nitrided Ge Surfaces, and Post-Deposition Annealing at 800°C**, ***G. Lucovsky***, *S. Lee, J.P. Long*, North Carolina State University, *J. Luening*, SSRL

Differences in length scales for nano-scale order in thin film nano-crystalline HfO_2 and TiO_2 deposited on i) remote plasma-nitrided Ge(100) substrates, and ii) Si(100) substrates with ultra-thin (~0.8 nm) SiON interfacial layers are addressed. Near edge X-ray absorption spectroscopy (NEXAS) is used to determine nano-scale order through the presence or absence Jahn-Teller (J-T) distortion removal of band-edge d-state degeneracies. These studies identify a new and novel application for NEXAS based on the resonant character of the respective N K_1 and O K_1 edge absorptions; these absorptions, respectively, provide a novel way to probe correlated changes in buried interfaces and nano-scale order for as-deposited and 800°C Ar annealed $HfO_2$and TiO_2 thin films. After an 800°C anneal, N K_1 edge spectra indicate an essentially complete elimination of interfacial GeN interfacial bonding on the Ge substrates, but no changes in SiON interfacial layer bonding on Si substrates. As-deposited films 2 nm, 4 nm and 6 nm thick on Ge and Si with interfacial transition regions do not display J-T splittings. This has been attributed to kinetically hindered nano-crystalline grain dimensions smaller than 2 nm. In contrast, after annealing, HfO_2 and TiO_2 films on Ge display spectroscopic evidence for J-T splittings, independent of film thickness. Annealed films on SiON interfaces display J-T splittings, but only for film thickness >3 nm in which grain size is not dimensionally constrained. The spectral signature of the J-T splittings for HfO_2 films on Ge is qualitatively different than for HfO_2 films SiON interfaces on Si. This is attributed to the TM oxide bonding directly to a Ge surface devoid of interfacial GeN serving as a template for mosaic in-plane controlled HfO_2 and TiO_2 grain growth to >3.5 nm. This grain size is sufficient to promote observable J-T spittings in O K_1 spectra. Equally significant, and consistent with the mosaic template description, the half-width-half-maximum of the O K_1 edge for annealed TiO_2 films is smaller for Ge substrates, 0.5 eV as compared with 0.6-0.7 eV for SiON interfaces on Si.

9:00am **EM-FrM4 Effect of Strain Localization and Percolation on Defect States by Controlled Nitrogen Incorporation in Hf Si Oxynitride Alloys**, ***S. Lee***, *G. Lucovsky, L.B. Fleming*, North Carolina State University, *J. Luning*, Stanford Synchrotron Radiation Laboratory

There are two qualitatively different ternary alloy regimes with markedly different properties that are obtained by incorporation of nitrogen in the form of Si_3N_4 bonding into TM silicates. These differentiated by i) strain localization and/or strain percolation, and more importantly iii) strain reduction associated with chemical bonding self-organizations that reduce macroscopic strain by more than compensating reductions in alloy atom entropy. In order to realize strain minimization, compositional optimization by remote plasma process processing was utilized for deposition of Hf, Ti and Hf,Ti alloy Si oxynitride dielectrics. For example, the effect of Si_3N_4 content in $(HfO_2)_x(Si_3N_4)_y(SiO_2)_{1-x-y}$ pseudo-ternary alloys has been studied spectroscopically, and also shows systematic changes in electrical properties, including reduction of electrically-active traps, and minimization of tunneling leakage. Results from soft X-ray photoelectron spectroscopy (SXPS) valence band studies indicate no detectable hole traps for Hf Si oxynitrides with Si_3N_4 content ~35 - 40%, and with equal concentrations of HfO_2 and SiO_2, ~30-32%. These alloys show no evidence for chemical phase separation, as do Hf silicates, and other Hf Si oxynitride compositions. Optimized alloys are stable to at least 1100°C annealing. Derivative near edge x-ray absorption spectroscopy (NEXAS) comparisons for O K1 edges of HfO_2 and optimized Hf Si oxynitride alloys display significantly decreases in electron trapping. The unique properties of optimized Hf Si oxynitrides are correlated with a four-fold coordination of Hf, in contrast with the 7-fold coordination of Hf in HfO_2. C-V measurements indicate a dielectric constant of ~12 in optimized Hf Si oxynitrides, and a predicted value of 16-18 in Hf,Ti Si oxynitrides. Combined with low electron trapping similar to SiO_2, and more than a 4 order of magnitude reduction in tunnel leakage, optimized TM Si oxynitride alloys are predicted to yield EOTs <1 nm, and possibly as low as 0.6 to 0.5 nm for aggressively scaled CMOS devices.

9:20am **EM-FrM5 A Comparison of the Nucleation and Growth of HfO_2 Thin Films Deposited by ALD Using TEMAH and TDMAH Precursors**, ***J.C. Hackley***, UMBC, *J.D. Demaree*, Army Research Laboratory, *T. Gougousi*, UMBC

A hot wall Atomic Layer Deposition (ALD) flow reactor has been used for the comparison of two different HfO_2 ALD chemistries: tetrakis (ethylmethylamino) hafnium (TEMAH) and H_2O, and tetrakis

(dimethylamino) hafnium (TDMAH) with H_2O on H-terminated Si and SC1 chemical oxide starting surfaces. Spectroscopic ellipsometry (SE) confirms linear growth of the films with a growth rate of ~1.2 Å/cycle at 250°C for the TEMAH process, and ~1.0 Å/cycle at 275°C for the TDMAH process. Nucleation and initial growth behavior of the films were examined using x-ray photoelectron spectroscopy (XPS) and Rutherford backscattering spectrometry (RBS). RBS indicates an initial 4-7 cycle nucleation barrier for the Si-H surface with both metal-organic precursors, before the growth rates on that surface match those on SC1. Steady-state coverage is attained after a 'conditioning' period of about 45 ALD cycles for TEMAH, as opposed to only 20 cycles with TDMAH. However, TEMAH results in a higher steady-state coverage rate of $3.1\text{x}10^{14}$ Hf/cm^2 on both starting surfaces, compared to $2.4\text{x}10^{14}$ Hf/cm^2 and $2.7\text{x}10^{14}$ Hf/cm^2 for the Si-H and SC1 surfaces with TDMAH. A comparison of the growth rate measurements with RBS and SE indicates that the HfO_2 films grown from TEMAH appear to reach about 85% of their bulk density on both starting surfaces while TDMAH results in 85% bulk density for the Si-H surface and 95% density on the SC1 surface. XPS is implemented to examine the Si/HfO_2 interfacial region for films grown on the Si-H starting surface. Angle-resolved scans ranging from 0-60° (measured from the surface normal) are taken for samples prepared with both precursors, ranging from 4-25 ALD cycles. For the TEMAH films, we detect a ~7 Å SiO_x/silicate interfacial layer which remains practically unchanged up to 50 ALD cycles as indicated by HRTEM data. In the TDMAH/H_2O process, the interface appears to be initially unstable, and the interfacial layer increases from ~6 Å at 4 cycles up to ~18 Å at 25 cycles. This unstable interface may be due to a more porous film structure, and/or the slightly higher deposition temperature than that of the TEMAH process (275 vs. 250 °C) which may enhance interface oxidation.

9:40am **EM-FrM6 Material Characteristics and Electrical Properties of Hafnium Silicate Films Synthesized by Plasma Enhanced Atomic Layer Deposition***, J.R. Liu, R.M. Martin,* ***M. Sawkar****, J.P. Chang*, University of California at Los Angeles

Pseudo-binary $(HfO_2)_x(SiO_2)_{1-x}$ has attracted much attention due to the interesting possibility of combining the high breakdown field of SiO_2 (E_g = 9 eV) and high dielectric constant (22~25) of HfO_2 in a complex material to keep a relatively high dielectric constant and a low leakage current.[1,2] In this work, $(HfO_2)_x(SiO_2)_{1-x}$ composite films were deposited from hafnium tetra-tert-butoxides (HTB) and tetraethylorthosilicate (TEOS) precursors by using an plasma-enhanced atomic layer deposition (PEALD) process. The film thickness increased almost linearly with increasing number of precursor-oxygen plasma cycles. An optimal control over the final composition was achieved by setting the deposition cycles of HfO_2 and SiO_2. Fourier Transform Infrared spectroscopy (FTIR) and x-ray photoelectron spectroscopy (XPS) analysis showed that the composite films were fully oxidized. The Si-O-Hf bonds were formed in the PEALD deposited composite films. The band gap determined from the XPS O 1s plasmon loss spectrum increased from 5.6 to 5.98 eV with increasing the Si content in the as-deposited films, and it increased slightly after the composite films were annealed at 600 and 900ºC, respectively. Time-of-flight static secondary ion mass spectrometry (TOF-SSIMS) depth profiles showed that Hf is almost uniformly distributed throughout the films, and Hf and O exhibited a sharp decay at the Si interfacial substrate. Some Hf presence at the interface with Si could be attributed to ion beam-induced mixing of Hf into the interfacial layer. The low carbon content in these films, which is confirmed by XPS, resulted from the ambient surface contamination. The as-deposited and annealed films at 900ºC were determined to be amorphous by x-ray diffraction (XRD), suggesting that the introduction of SiO_2 into HfO_2 matrix prevented crystallization and kept the film amorphous at high temperature. The as-deposited $(HfO_2)_x(SiO_2)_{1-x}$ composite films showed superior electrical properties, including dielectric constants from 5.3 to 11.5 and leakage current density several orders of magnitude lower than that of SiO_2 at the same equivalent oxide thickness.

[1] R. M. Wallace and G. Wilk, MRS Bulletin, 192, 27 (2002).
[2] R. Puthenkovilakam, M. Sawkar, and J. P. Chang, Appl. Phys. Lett., 202902, 86 (2005).

10:00am **EM-FrM7 Band Alignment in Metal/Oxide/Semiconductor Stacks***,* ***S. Rangan****, E. Bersch, R.A. Bartynski, E. Garfunkel*, Rutgers University

Understanding band alignment in a Metal/Oxide/Semiconductor (MOS) structure is both a fundamental physical chemistry challenge and a crucial technological issue for nanoelectronics as the correct band offsets across a MOS stack is essential to prevent undesirable leakage currents in device applications. A recurrent problem in the evaluation of the band offsets is the lack of reproducibility between measurements on nominally identical samples and between measurements performed using different experimental methods. In this study, we have performed ultra-violet photoemission and inverse photoemission spectroscopy measurements in the same UHV system on a variety of high-κ dielectric films (HfO_2, $Hf_{0.8}Si_{0.2}O_2$, SiO_2, Al_2O_3, ZrO_2) on different semiconductor substrates (Si, Ge, GaAs). This experimental setup allows the direct determination of band gaps, electron affinities, metal work functions, and band offsets across MOS structures. We have also explored the effect of subsequent metallization of the high-κ film in UHV with either of metals (Ru, Ti, Al) chosen for their very different work function and oxygen affinity. By examining the line shape of the shallow core levels using synchrotron radiation-excited x-ray photoemission spectroscopy, we determined the chemical state of the metal, the oxide and the substrate. Ru and Ti are found to remain metallic upon deposition on all oxide films used in this study. In contrast, strong changes in the chemistry of the entire stack are observed upon Al deposition. An Al_2O_3 interface layer is always present at the Al/Oxide interface, and evidence for reduction of the semiconductor/high-κ interface oxide is also observed. Consistent with the observed level of reactivity, our measured Metal/Oxide band offsets are in good agreement with the values predicted by the interface gap state model for as-deposited Ru and Ti. In the case of Al, owing to an additional Al_2O_3 interface layer between the oxide and the Al, our measured values are in poor agreement with the interface gap state model. This indicates that for reactive metal, the band offset is not well described by this simple model.

10:20am **EM-FrM8 Thermal Stability of Rare Earth Oxides as High-k Gate Dielectrics***,* ***S. Van Elshocht****, C. Adelmann, T. Conard, A. Delabie, A. Franquet,* IMEC vzw, Belgium*, P. Lehnen,* AIXTRON, Germany*, L. Nyns, O. Richard,* IMEC vzw, Belgium*, J. Swerts,* ASM Belgium*, S. De Gendt*, IMEC vzw, Belgium

Chip performance has drastically increased during the past decades, pushed forward by the ITRS roadmap that projects a doubling of the amount of transistors on a chip every two years. This task has been mainly accomplished by down scaling the dimensions of the transistor, including the gate dielectric thickness down to a few atomic layers. As a result, gate leakage current densities have reached unacceptable levels. As a solution alternative gate dielectrics, replacing the standard SiON, were researched, leading to the identification of Hf-based dielectrics, recently announced to be integrated in the 45-nm technology node. Another class of alternative dielectrics that receives a lot of attention is the rare earth oxides, both as binary or ternary compounds. Rare earth oxides are being explored for their property to shift the work function of a metal gate towards n-type, which is of interest to engineer a proper transistor threshold voltage. In addition, ternary rare earth oxides have been studied because of their thermal stability that allows obtaining a material that remains amorphous during the entire CMOS process. We have studied the thermal behavior and stability of rare earth based oxides, such as Dy_2O_3, La_2O_3, $LaAlO_3$, $HfLaO_x$, and $DyScO_3$, as function of anneal temperature, time, and ambient, as well as function of their composition. Observations were made by Spectroscopic Ellipsometry, Time-Of-Flight-Secondary Ion Mass Spectroscopy, Transmission Electron Microscopy, X-Ray Reflectometry, and X-Ray Diffraction. The rare earth oxide strongly intermixes with the SiO_2 layer underneath, in agreement with the tendency of rare earth elements to form silicates.[1] More interestingly, for ternary rare earth oxides, this behavior is heavily dependent on the composition of the deposited layer. The system evolves to a stable composition that is controlled by the thermal budget and the rare earth content of the layer. Understanding this behavior is important, since it provides a better insight in the behavior of these dielectrics during the thermal treatments inherent to a CMOS process flow. Finally, as an increased Si-content, resulting from silicate formation, can increase the thermal stability of a material, proper care needs to be taken interpreting thermal stability measurements, most often based on X-Ray Diffraction.

[1] H. Ono et al., Appl. Phys. Lett., 78, 1832 (2001).

10:40am **EM-FrM9 Diffusion of La-based Layers on HfO_2/SiO_2/Si Dielectric Stacks***, M.I. Medina-Montes,* The University of Texas at Dallas and Cinvestav-Queretaro, Mexico*, M.V. Selvidge, F.S. Aguirre-Tostado,* The University of Texas at Dallas*,* ***A. Herrera-Gomez,*** The University of Texas at Dallas and Cinvestav-Queretaro, Mexico*, R.M. Wallace*, The University of Texas at Dallas

Although there is a consensus regarding the use of Hf-based dielectrics as an alternative to SiO_2 in MOS structures, the search for a suitable metal for n-MOS is still open. The addition of a La-based layer to $Hf_xSi_{1-x}O_2/SiO_2$/Si dielectric stacks has proven to allow for the engineering of the work function to appropriate levels when TaN or TiN is employed as the metal gate. It has been suggested that the La diffuses into the Hf layer with thermal treatment. We performed high resolution Angle Resolved X-Ray Photoelectron Spectroscopy experiments to study the chemical depth profile distribution of $La_2O_3/HfO_2/SiO_2$/Si dielectric stacks exposed to a nitridation treatment by NH_3 at 700°C. The expected stoichiometry and distribution of the HfO_2 and SiO_2 layers was reproduced from self consistent analysis of the ARXPS data. Regarding La, this study clearly shows that it diffuses to the top of the SiO_2 layer, and that subsequent Rapid Thermal Annealing at 1000°C for 5s does not change significantly that distribution. A similar

conclusion was derived by Sivasubramani et al. from FTIR analysis.[1] In addition, back-side Secondary Ion Mass Spectroscopy results presented by Alshareef et al. are consistent with a location for La close to the HfO_2/SiO_2 interface.[2] The quantitative results for the location and amount of La, together with the associated uncertainties, will be discussed in extent in the presentation.

[1] P. Sivasubramani, T. S. Boscke, J. Huang, C. D. Young, P. D. Kirsch, S.A. Krishnan, M.A. Quevedo-Lopez, S. Govindarajan, B.S. Ju, H.R. Harris, D.J. Lichtenwalner, J.S. Jur, A.I. Kingon, J. Kim, B.E. Gnade, R.M. Wallace, G. Bersuker, B.H. Lee, and R. Jammy. VLSI (2007).

[2] H.N. Alshareef, M. Quevedo-Lopez, H.C. Wen, R. Harris, P. Kirsch, P. Majhi, B.H. Lee, R. Jammy, D.J. Lichtenwalner, J.S. Jur, and A.I. Kingon. Applied Physics Letters 89, p. 232103 (2006).

11:00am **EM-FrM10 Physical and Chemical Properties of Hf-based High-κ Dielectrics on Ge(001) for CMOS Applications**, *F.S. Aguirre-Tostado, M. Milojevic, S.J. McDonnell, M.J. Kim,* ***R.M. Wallace***, University of Texas at Dallas

The growth of High-κ dielectrics on Ge has attracted substantial interest as a means to maintain integrated circuit scaling and performance. High-κ dielectrics on Ge studies have shown promising results in terms of low equivalent oxide thickness[1] and enhanced hole mobility.[2,3,4] For MOSFET applications, the thermal stability of gate dielectrics is a requirement for an appropriate CMOS flow. This paper will describe the thermal stability studies of HfGeON gate dielectrics on Ge for several nitrogen concentrations. The structure and chemistry of the HfGeON/Ge(001) layers are studied using HRTEM, XRD and in-situ XPS and LEISS. Sputter deposited HfGeON films on atomically clean Ge epi-layers grown by MBE on Ge(001) substrates are investigated. Corresponding electrical characterization of the associated devices will also be described in view of the thermal budget where the maximum process temperature is ~500°C. This work is supported by the MARCO MSD Focus Center.

[1]C.O. Chui, S. Ramanathan, P.C. McIntyre, and K.C. Saraswat, IEEE Elec. Dev. Lett. 23, (2002) 473.

[2]C. H. Huang, et. al., in Symp. VLSI Tech. Dig., 2003, pp. 119-120.

[3]C. Chui, H. et.al., in IEDM Tech. Dig., Dec. 2002, pp. 437-440.

[4]W. P. Bai, et.al., in Symp. VLSI Tech. Dig., 2003, pp. 121-122.

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